AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device with an MOS transistor, wherein a gate electrode of the MOS transistor is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer, wherein the metal silicide layer and the metal nitride layer are formed as individual layers to function as a contact resistance reducing layer and as a reaction barrier layer, respectively, and wherein said metal silicide layer has a thickness of 5 to 20 nm.

2. (Previously Presented) A semiconductor device according to Claim 1, wherein the silicon layer is doped with an impurity of any desired conductivity type.

3. (Canceled).

4. (Previously Presented) A semiconductor device according to Claim 1, wherein the metal silicide layer is a tungsten silicide layer, the metal nitride layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

5. (Currently Amended) A semiconductor device with an MOS transistor whose gate electrode is provided as a stacked structure comprising a silicon layer and a metallic layer as the uppermost layer thereof, wherein a metal silicide layer is provided on the silicon layer side and a metal nitride layer is provided under the metallic layer side between the silicon layer and the metallic layer, wherein the metal silicide layer and the metal nitride layer are formed as individual layers to function as a contact resistance reducing layer and as a reaction barrier layer, respectively, and wherein said metal silicide layer has a thickness of 5 to 20 nm.

6. (Previously Presented) A semiconductor device according to Claim 5, wherein the silicon layer is doped with an impurity of any desired conductivity type.

7. (Canceled).

8. (Previously Presented) A semiconductor device according to Claim 5, wherein the metal silicide layer is a tungsten silicide layer, the metal nitride layer is a tungsten nitride layer and the metallic layer is a tungsten layer.

Claims 9-16 (Canceled).

17. (Previously Presented) A semiconductor device according to claim 1, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

18. (Previously Presented) A semiconductor device according to claim 4, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

19. (Canceled).

20. (Previously Presented) A semiconductor device according to claim 1, wherein the gate electrode is provided above a principal surface region of a semiconductor substrate, covering the spacing between a source region and drain region of the MOS transistor, the source and drain regions each having a first diffusion layer and a second diffusion layer, the second diffusion layer having a junction depth extended into the substrate deeper than that of the first layer.

21. (Previously Presented) A semiconductor device according to claim 20, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

22. (Previously Presented) A semiconductor device according to claim 5, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

23. (Previously Presented) A semiconductor device according to claim 8, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

24. (Canceled).

25. (Currently Amended) A semiconductor device with complementary MOS transistors, each MOS transistor having a gate electrode, a source region and a drain region, wherein the gate electrode is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer, wherein the metal silicide layer and the metal nitride layer are formed as individual layers to function as a contact resistance reducing layer and as a reaction barrier layer, respectively, and wherein said metal silicide layer has a thickness of 5 to 20 nm.

26. (Previously Presented) A semiconductor device according to claim 25, wherein the silicon layer of each MOS transistor gate electrode is a polycrystalline silicon layer doped with an impurity of one of an n-type and p-type conductivity for the gate electrode of a n-channel type MOS transistor and doped with an impurity of the other one of the n-type and p-type conductivity for the gate electrode of a p-channel type MOS transistor.

27. (Canceled).

28. (Previously Presented) A semiconductor device according to claim 25, wherein the metal silicide layer is a tungsten silicide layer, the metal nitride layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

29. (Currently Amended) A semiconductor device with complementary MOS transistors, each MOS transistor having a gate electrode, a source region and a drain region, wherein the gate electrode is provided as a stacked structure comprising a silicon layer, an uppermost metallic layer, a metal silicide layer provided on the silicon layer side and a metal nitride layer provided under the metallic layer side between the silicon layer and the metallic layer, wherein the metal silicide layer and the metal nitride layer are formed as individual layers to function as a contact resistance reducing layer and as a reaction barrier layer, respectively, and wherein said metal silicide layer has a thickness of 5 to 20 nm.

30. (Previously Presented) A semiconductor device according to claim 29, wherein the silicon layer of each MOS transistor gate electrode is a polycrystalline silicon layer doped with an impurity of one of an n-type and p-type conductivity for the gate electrode of a n-channel type MOS transistor and doped with an impurity of the other one of the n-type and p-type conductivity for the gate electrode of a p-channel type MOS transistor.

31. (Previously Presented) A semiconductor device according to claim 29, wherein the metal silicide layer is a tungsten silicide layer, the metal nitride layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

32. (Canceled).

33. (Currently Amended) A semiconductor device comprising, on a substrate, at least one MOS transistor, wherein a gate electrode of the MOS transistor is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer, wherein the metal silicide layer and the metal nitride layer are formed as individual layers to function as a contact resistance reducing layer and as a reaction barrier layer, respectively, and wherein said metal silicide layer has a thickness of 5 to 20 nm .

34. (Previously Presented) A semiconductor device according to Claim 33, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

35. (Canceled).

36. (Previously Presented) A semiconductor device according to Claim 33, wherein said substrate includes a semiconductor substrate.

37. (Previously Presented) A semiconductor device according to Claim 33, wherein the gate electrode is provided above a principal surface region of a semiconductor substrate, covering the spacing between a source region and drain region of the MOS transistor, the source and drain regions each having a first diffusion layer and a second diffusion layer, the second diffusion layer having a junction depth extended into the substrate deeper than that of the first layer.

38. (Previously Presented) A semiconductor device according to Claim 37, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

39. (Canceled).

40. (Previously Presented) A semiconductor device according to Claim 37, wherein said substrate includes a semiconductor substrate.